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EXAMINER

HASSAN, AURANGZEB

ART UNIT	PAPER NUMBER
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2182

MAIL DATE	DELIVERY MODE
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06/04/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/697,996

Applicant(s)

HOMEWOOD ET AL.

Examiner

Aurangzeb Hassan

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

~~3-30~~
3-30

- 4) ☒ Claim(s) 1, 2 and 30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/6/07 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show any functional description, other than black boxes left for interpretation, as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the

remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 26, 27 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not provide enablement to the newly amended claim limitations as to how a stream engine sends a stall signal based upon a FIFO that is internal to the stream register unit. The FIFO in the specification is located in the system, external to the stream register unit, not in the stream register unit itself. Consequently enablement is lacking as to how a stream engine is capable of receiving requests, making determinations therein, and transmitting stalls and interrupt based on a predetermined period of time. The specification at best hints at stream engine functionality in the Background/Field of Invention section paragraphs 9 and 10. There is no evidence as to how this function can work with an internal FIFO; therefore one skilled in the art would not be able to carryout the claim limitations as recited in the instant application without undue experimentation.

To expedite complete examination of the instant application, the Examiner will best interpret the claim limitations outlining the stream engine to recite the alternative obvious variant of the enable instance where the FIFO is external to the stream register unit as seen in claims 1 and 11 and as claimed in the previously presented claims 26, 27 and 30 dated 8/9/2006 in light of paragraphs [009-0010].

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 11, 15, 19, 26 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 11 and 15 recite "stream register unit is arranged to ... send ... to the processor". In light of the newly amended claim limitations from which claims 11 and 15 depend it is unclear to the Examiner as to how a stream register unit, which is part of the processor, can send signals to the processor, i.e. processor sending signals to itself.

8. Claim 19 recites the limitation "the stream register" in line 3. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 26 and 30 recite in the preamble a structural relationship for a processor, stream register unit and a peripheral/memory. The claims necessitate that the stream

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register unit is between a processor and a memory yet at the same time the stream register unit is part of the processor. It is unclear to the Examiner how the stream register unit can be itemized as externally between a processor and peripheral/memory yet at the same time be internal to the processor.

In order to expedite complete prosecution of the instant application the Examiner will best interpret the claim limitations of the preamble to recite the preamble that was proper in the previous presentation, "stream register connectable between a processor and" (claim 26, lines 1 and 2, dated 8/9/2006).

Clarification/correction required.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1, 3 – 9, 13 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis et al (U.S. Patent No. 5,797,043 hereinafter "Lewis") in view of George et al. (US Patent Number 6,785,829, hereinafter "George").

12. As to Claims 1 and 24, Lewis teaches a system comprising:

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a processor for executing instructions; (Host Processor, element 12, figure 1a)

a stream register unit configured to supply a first type of data to the processor, the first type of data being data supplied from a peripheral (I/O Channel Controller, element 62, figure 3, element 140, figure 5a), the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral (FIFO pool 172, figure 5a);

a FIFO coupled to the peripheral to receive said first type of data from the peripheral (column 14, lines 25 – 29) and connected to the stream register unit by a communication path (FIFO Pool Bus 144, figures 5a and 6), along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6); and

a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access the second type of data, the second type of data being randomly accessible data held in the data memory (Processor Bus, element 16', figure 2).

Lewis fails to teach a system wherein a stream register unit being part of the processor.

George teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3).

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It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of George. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing.

13. As to claim 3, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit accordance with requests for data made (requested function, column 13, 23 – 30) by the processor to the stream register unit and forwarded to the FIFO (FIFO pool buffering functions, column 12, lines 38 –58).

14. As to claim 4, Lewis teaches a system, wherein the said requests are made as accesses to volatile variables (10 Bit – Request variable changes consistently per requested lines of data and can be changed at any time, Table VIII).

15. As to claim 5, Lewis teaches a system wherein the FIFO is arranged to, upon receiving a request for data from the stream register unit, send a signal to the stream register unit indication availability of the requested data (available space and data, Table VII sent via BTU, element 170 figure 5b.).

16. As to claim 6, Lewis teaches a system, wherein if the FIFO contains the requested data, the said signal to the stream register unit indicates that the data is

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available, and the FIFO is further arranged to send (burst data transfer, column 20, lines 1 – 4) a signal (transfer signals, Table VI) to the stream register unit comprising the data (column 19, lines 64 – 67, column 20, lines 1 – 35).

17. As to claim 7, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, supply the data (data stream, element 76, figure 3) to the processor (column 10, lines 25 – 41, passed to DSP, column 20 lines 5 - 35).

18. As to claim 8, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, send a signal to the FIFO indicating that it has taken the data (Transfer Done, Table VII).

19. As to claim 9, Lewis teaches a system, wherein the said signal to the FIFO further indicates the next location in the FIFO from which the data is required (next sequential, column 16, lines 10 – 33).

20. As to claims 13 and 25, Lewis teaches a system, further comprising a timeout generator, arranged for communication with the processor and the stream register unit, and arranged to, if the signal sent by the FIFO is a signal indicating that the data is not available (data available in the FIFO, Table VIII), after a predetermined period of time,

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send a timeout signal to the processor, causing the processor to interrupt (Interrupt, Table III & XXIV) such that it can execute other instructions (column 36, lines 1 – 17).

21. As to claim 14, Lewis teaches a system, wherein if following sending of the timeout signal to the processor the data subsequently becomes available, the timeout generator is arranged to receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal (column 36, lines 18 – 40).

22. As to claim 15, Lewis teaches a system, wherein the stream register unit is arranged to, if following sending of the timeout signal to the processor the data subsequently becomes available, send the data to the processor (in response to host interrupts, the host processor provides for the transfer of data, column 26, lines 25 – 34).

23. As to claim 16, Lewis teaches a system, wherein the stream register unit is associated with a register file containing a plurality of registers (register based interface, column 22, lines 15 – 33) and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63).

24. As to claim 17, Lewis teaches a system, wherein the processor is arranged to retrieve data from the register file (column 22, lines 15 – 33).

25. As to claim 18, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit in accordance with requests for data made by the processor to the stream register unit and forwarded to the FIFO (figure 1a and 1b), wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63), wherein the processor is further arranged to make requests for data to the stream register unit via the load/store unit (column 33, lines 33 – 39).

26. As to claim 19, Lewis teaches a system, wherein the stream register unit comprises one or more FIFOs connected to receive data from the FIFO connected to the stream register and supply the data to the processor (FIFO 0 – 3, elements 210 – 212, figure 5c).

27. As to claim 20, Lewis teaches a system, wherein the request for data is a request for a single data item (column 10, lines 30 - 41).

28. As to claim 21, Lewis teaches a system, further comprising one or more additional FIFOs linked (FIFO 0 – 3, elements 210 – 212, figure 5c) together between the said FIFO and the communication channel (FIFO pool subsystem, figure 6).

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29. As to claim 22, Lewis teaches a system, wherein the data from the peripheral is video data (video words, column 25, lines 37 – 40).

30. As to claim 23, Lewis teaches a system, wherein the peripheral is a video processing system (video controller, column 25, lines 29 – 48).

31. Claims 10 thru 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of George further in view of Lai et al. (US Patent Number 6,433,785 hereinafter “Lai”).

32. As to claim 10, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

The combination of Lewis and George fails to teach system wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available.

Lai teaches a system, wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available (first defer identifier, column 3, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request

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process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

33. As to claim 11, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

The combination of Lewis and George fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

Lai teaches a system, wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions (issue a stop signal, column 3, lines 20 - 26).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system.

34. As to claim 12, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

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The combination of Lewis and George fails to teach system wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit.

Lai teaches a system, wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit (when the initiator is ready, data transfer between the initiator and the responder begins, column 3, lines 32 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system requesting data.

35. Claim 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785 hereinafter “Garcia”).

(As best interpreted in light of the 35 U.S.C. 112 rejection above, clarification/correction required)

36. As per claims 26 and 30, Lewis teaches a stream register connectable between a processor and peripheral and between a processor and a memory, comprising:

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a receiver arranged to receive a request for a data item from the processor (column 10, lines 30 - 41); at least one FIFO configured to store the data item received from the peripheral (FIFO pool 172, figure 5a); and

a stream engine (element 76, figure 3), arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item (I/O Channel Controller, element 62, figure 3), and, if the data item is available (available space and data, Table VII sent via BTU, element 170 figure 5b.), send the data item to the processor.

Lewis fails to teach a register wherein if the data item being requested is not available, sending a timeout signal to the processor.

Garcia teaches a register wherein if the data item being requested is not available, sending a timeout signal to the processor (timeout counter, column 5, lines 26 – 42)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Garcia. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

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37. As to claim 27, Lewis teaches a stream register, wherein the stream engine is arranged to the interrupt signal to the processor after a predetermined period of time (Interrupt, table III).

38. As to claim 28, Lewis teaches a stream register, wherein the stream engine is further arranged to, if the data is available, temporarily store the data in a register file for access by the processor (temporarily stored in a FIFO within the bus master units, column 19, lines 52 – 63).

39. Lewis modified by the teachings of Garcia as applied to claims 26 and 30 above, in regards to claim 29, Lewis teaches a stream register, wherein the stream engine is further arranged to temporarily store (column 19, lines 52 – 63) the data in a register file for access by the processor (column 18, lines 29 – 36).

Lewis fails to teach a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data item subsequently becomes available, receive a signal instructing it to cease sending the timeout signal, and to upon receipt of the said instruction cease sending the timeout signal to the processor.

Garcia teaches a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data item subsequently becomes available (posted write buffer available signal 350, column 5, lines 30 – 31), receive a signal instructing it to cease sending the timeout signal, and to

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upon receipt of the said instruction cease sending the timeout signal to the processor (column 5, lines 26 – 42).

Response to Arguments

40. Applicant's arguments with respect to claims 1, 3 – 9, 13 – 30 have been considered but are moot in view of the new ground(s) of rejection.

All of the Applicant's arguments are directed to newly amended claim limitations, which are addressed in the rejection above. Applicant is further directed to note 35 U.S.C 112 first and second paragraph rejections as they also pertain to the newly amended claims.

Conclusion

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH



KIM HUYNH
SUPERVISORY PATENT EXAMINER

5/23/07